REMARKS/ARGUMENTS

Claims 1-44 are pending in this application, Claims 1, 14-16, 22, 43 and 44 are amended.

The Examiner has not acknowledged receipt of the IDS that was filed on **October 16, 2000**. Applicants respectfully submit that the above IDS was filed on **October 16, 2000** with legible copies of all the cited references. Applicants respectfully request acknowledgment of the IDS by initialing and returning the attached copy of the same IDS. If the Examiner still cannot locate the copies submitted on October 16, 2000, in the file, the undersigned attorney respectfully requests the courtesy of a telephone call so that he could provide the Examiner with new copies of the requested references.

Claims 1-9, 19-30 and 41-44 are rejected under 35 U.S.C. 103(a) as being obvious over Tseng et al. (U.S. Patent 6,009,256) in view of Schlansker et al. (U.S. Patent 6,408,428), and further in view of Kolchinsky et al. (U.S. Patent 5,535,406). Applicants submit that all of the pending claims are patentable over the cited references, and reconsideration and allowance of the pending claims are respectfully requested.

Amended independent claims 1, 43 and 44 include, among other limitations, "identifying a plurality of functions in a program source code that are anticipated to consume a substantial execution time," and "decomposing the program source code into a plurality of kernel sections, wherein the identified plurality of functions are recognized as the plurality of kernel sections." Applicants respectfully submit that the cited

references alone or in combination do not disclose or suggest the recited limitation.

Rather, the system of Tseng generates hardware models for pre-classified components (such as, combinational components and register components) in a netlist. For example, Tseng clearly states that "Step 302 performs component type analysis by classifying HDL components into combinational components, register components, clock components, memory components, and test-bench components as shown in component type resource 303. The SEmulation system generates hardware models for register and combinational components, with some exceptions as discussed below. Test-bench and memory components are mapped in software. . . . Combinational components are stateless logic components whose output values are a function of current input values and do not depend on the history of input values. . . . Register components are simple storage components. The state transition of a register is controlled by a clock signal. One form of register is edge-triggered which may change states when an edge is detected." (Col. 17, lines 24-45, underlining added.)

Furthermore, Tseng describes how the system performs the component type analysis by stressing that "[t]he system examines the binary source design database. Based on the source design database, the system can characterize or classify the elements as one of the above component types. Continuous assignment statements are classified as combinational components. Gate primitives are either combinational type or latch form of register type by language definition. Initialization code are treated as test-benches of initialization type. An always

process that drives nets without using the nets is a test-bench of driver type. . . " (Col. 18, lines 21-30, underlining added.)

Consequently, the system of Tseng identifies pre-classified component types (i.e., combinational and register components) and then generates hardware models for only those pre-classified component types.

In contrast, the present invention, as claimed by the amended claims 1, 43 and 44 identifies "a plurality of functions in a program source code that are anticipated to consume a substantial execution time," and decomposes "the program source code into a plurality of kernel sections, wherein the identified plurality of functions are recognized as the plurality of kernel sections." These kernel sections are then mapped "into a plurality of hardware dependent executable code for execution on the plurality of hardware accelerators."

In fact, by only generating hardware models for the combinational and register components that are relatively simple components (see, e.g., col. 17, lines 35-42, cited above), the system of Tseng teaches away from "identifying a plurality of functions in a program source code that are anticipated to consume a substantial execution time," as recited by the amended independent claims 1, 43 and 44.

Schlansker discloses a system for designing a VLIW processor using feedback about internal resource utilization by reading a specification of a candidate VLIW processor, which describes a specific instance of a parameterized processor design. The system then obtains internal resource usage

statistics for the candidate processor. Thus, Schlansker, alone or in combination with Tseng, does not teach or suggest "identifying a plurality of functions in a program source code that are anticipated to consume a substantial execution time," and "decomposing the program source code into a plurality of kernel sections, wherein the identified plurality of functions are recognized as the plurality of kernel sections," recited by the independent claims 1, 43 and 44.

Kolchinsky describes a virtual processor with a reconfigurable, programmable logic array for processing data in accord with a hardware encoded algorithm. Likewise, Kolchinsky, alone or in combination with Tseng and/or Schlansker, does not teach or suggest "identifying a plurality of functions in a program source code that are anticipated to consume a substantial execution time," and "decomposing the program source code into a plurality of kernel sections, wherein the identified plurality of functions are recognized as the plurality of kernel sections," as recited by the independent claims 1, 43 and 44.

Applicants therefore respectfully submit that independent claims 1, 43 and 44 are novel and unobvious over the cited references and are therefore allowable.

Amended independent claim 22 includes, among other limitations, "a plurality of kernel sections identified as the functions that are anticipated to consume a substantial execution time in a program source code, for execution on said plurality of hardware accelerators." As discussed above, Applicants respectfully submit that independent claim 22 is also

novel and unobvious over the cited references and is therefore also allowable.

Applicants further submit that claims 2-21 and 23-42 that depend directly or indirectly from claims 1 and 22, respectively are allowable as are claims 1 and 22, and for additional limitations recited therein.

For example, dependent claims 15 and 36 include the additional limitation of "identifying functions [sections, in claim 36] with a limited number of inputs and outputs." None of the cited references, alone or in combination teach or suggest this limitation. Applicants respectfully disagree with the statement in the Office action (page 13, first paragraph) that the register component types of Tseng are fetched from the component type analysis because their "inputs and outputs connections are in very limited number." As explained above, the system of Tseng identifies pre-classified component types (i.e., register components) and generates hardware models for only those pre-classified component types, and not based on "a limited number of inputs and outputs," as required by the dependent claims 15 and 36. Therefore, dependent claims 15 and 36 are also allowable over the cited references as are their respective base claims 1 and 22, and for additional limitations recited therein.

As another example, dependent claims 16 and 37 include the additional limitation of "identifying functions [sections, in claim 37] with a limited number of branches." None of the cited references, alone or in combination teach or suggest this limitation. Applicants respectfully disagree with the statement

in the Office action (page 13, second paragraph) that the register component types of Tseng (alleged basic blocks) are fetched from the component type analysis because they include "a limited number of branches." As explained above, the system of Tseng identifies pre-classified component types (i.e., register components) and generates hardware models for only those pre-classified component types, and not based on "a limited number of inputs and outputs," as required by the dependent claims 15 and 36. Accordingly, dependent claims 16 and 37 are also allowable over the cited references as are their respective base claims 1 and 22, and for additional limitations recited therein.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application is now in condition for allowance, and accordingly, reconsideration and allowance are respectfully requested.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

By _____
Raymond R. Tabandeh
Reg. No. 43,945
626/795-9900

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Attorney's Docket No. 03048.P008

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:

Christopher Songer, et al.

Application No.: 09/651,425

Filing Date: August 30, 2000

For: SYSTEM AND METHOD FOR PREPARING SOFTWARE FOR EXECUTION IN A DYNAMICALLY CONFIGURABLE HARDWARE ENVIRONMENT

Examiner: Not Assigned

Art Unit: Not Assigned

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Washington, D.C. 20231

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Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

This Information Disclosure Statement is being submitted pursuant to 37 C.F.R. §1.97(b). If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 16 October 2000

Dennis A. Nicholls
Reg. No. 42,036

12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA 90025-1026 (408) 720-8300

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	09/651,425
Filing Date	August 30, 2000
First Named Inventor	Christopher Songer
Group Art Unit	Not Assigned
Examiner Name	Not Assigned
Attorney Docket Number	03048.P008

U.S. PATENT DOCUMENTS

Examiner Initials *		U.S.Patent Document Number	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Filing Date if Appropriate
		6,122,719	Mirsky		
		5,915,123	Mirsky		
		6,108,760	Mirsky		
		5,742,180	DeHon et al.		
		4,967,340	Dawes		
		5,956,518	DeHon et al.		

FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS

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		"Smart Compilers Puncture Code Bloat," Brown, Electronic Engineering Times, October 9, 1995 (pages 38 & 42).	
		"A High-Performance Microarchitecture with Hardware-Programmable Functional Units," Razdan et al., Micro-27 Proceedings of the 27th Annual International Symposium on Microarchitecture, 11/30-12/2/94 (pp. 172-180).	
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		"Coarse-Grain Reconfigurable Computing," Mirsky, Ethan A., Thesis submitted at the Massachusetts Institute of Technology, June 1996.	

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Application Number	09/651,425
Filing Date	August 30, 2000
First Named Inventor	Christopher Songer
Group Art Unit	Not Assigned
Examiner Name	Not Assigned
Attorney Docket Number	03048.P008

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		"SOP: Adaptive Massively Parallel System," by Tsukasa Yamauchi et al., NEC Research & Development, Vol. 37, No. 3, July 1996 (pp. 382-393).	

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